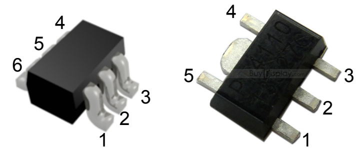
PWM CONTROL STEP-UP SWITCHING REGULATOR

FEATURES

- Low Start-up Input Voltage: 0.9V @ I_{OUT} = 1mA
- 1MHz Fixed Switching Frequency
- 90% Efficiency
- High Supply Capability to Deliver 3.3V/300mA with One Alkaline Cell or Deliver 5V/1.1A with One Li-ion Cell
- 17μA Quiescent (Switch-off) Supply Current
- 0.01μA Shutdown Mode Supply Current
- Providing Flexibility for Using Internal Power Switches
- Output Voltage: Settable to Between 2.0V to 6.0V, Accuracy of 2%

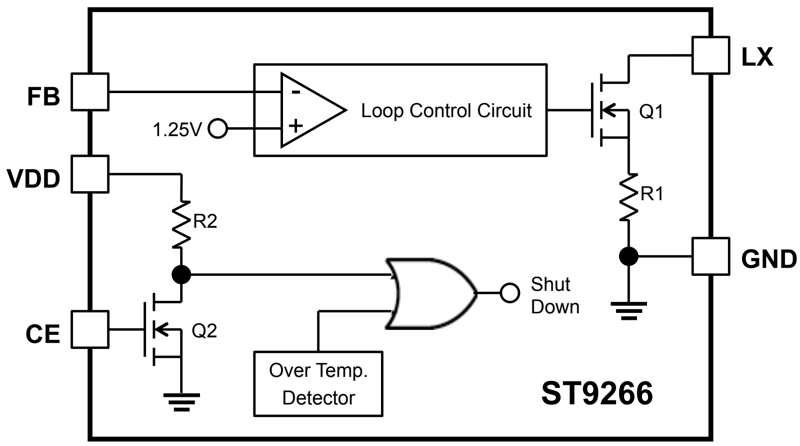


SOT-23-6L SOT-89-5

DESCRIPTION

The ***STComponet*** ST9266 is a compact, high efficiency, and low voltage step-up DC/DC converter with an Adaptive Current Mode PWM control loop, includes an error amplifier, ramp generator, comparator, switch pass element and driver in which providing a stable and high efficient operation over a wide range of load currents. It operates in stable waveforms without external compensation.
The low start-up input voltage below 0.9V makes ST9266 suitable for 1 to 4 battery cells applications of providing up to 1.1A output current. Besides, the 17μA low quiescent current together with high efficiency maintains long battery lifetime. The output voltage is set with two external resistors.

INTERNAL SCHEMATIC DIAGRAM



DEVICE SUMMARY

Ordering Code	Pin Configuration						V_{FB} Accuracy	Package Type	Shipping	Marking [1]
	CE	NC	GND	LX	VDD	FB				
ST9266A1MR	1	2	3	4	5	6	±1%	SOT-23-6L	Taping reel	AA1X
ST9266A2MR	1	2	3	4	5	6	±2%	SOT-23-6L	Taping reel	AA2X
ST9266A1PR	1	-	5	4	2	3	±1%	SOT-89-5	Taping reel	A X A 1
ST9266A2PR	1	-	5	4	2	3	±2%	SOT-89-5	Taping reel	A X A 2

Note 1: **X**: Assembly lot number: 0 ~ 9, A ~ Z mirror writing. (G, I, J, O, Q, W exception)

ABSOLUTE MAXIMUM RATINGS [2]

T_A = 25°C, all voltages respect to ground unless otherwise specified.

PARAMETER		SYMBOL	RATINGS	UNIT
Input Voltage		V_{DD}	-0.3 ~ +7	V
Output Voltage		V_{OUT}	-0.3 ~ +7	V
		V_{LX}	-0.3 ~ +7	V
LX Pin Switch Current		I_{LX}	2.5	A
Power Dissipation	SOT-23-6L	P_D	150	mW
	SOT-89-5		500	mW
Operating Ambient Temperature		T_{opr}	-40 ~ +80	°C
Storage Temperature Range		T_{stg}	-65 ~ +150	°C

Note 2: Absolute Maximum Ratings are those values beyond which the device could be permanently damaged. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Thermal Data

PARAMETER		SYMBOL	RATINGS	UNIT
Thermal Resistance, Junction-to-Case	SOT-23-6L	$R_{\theta JC}$	145	°C/W
	SOT-89-5		45	

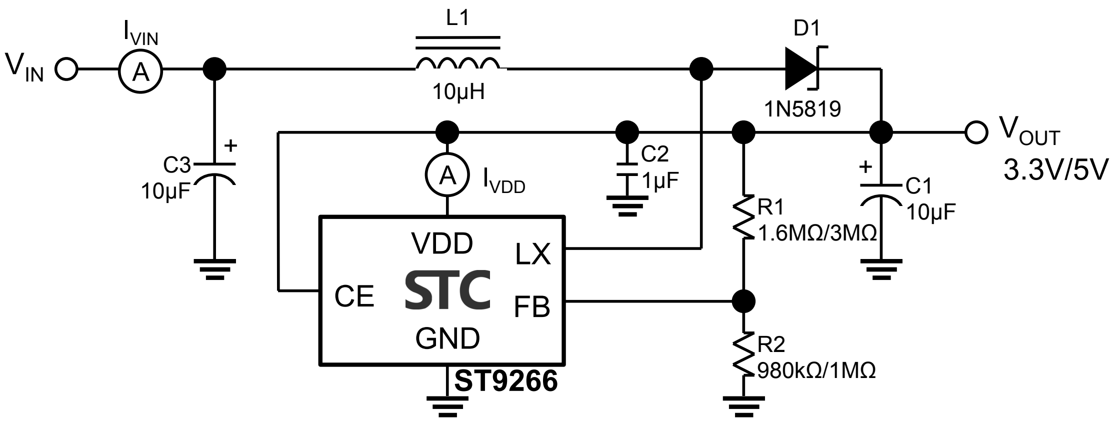
ELECTRICAL CHARACTERISTICS

V_{IN} = 1.5V, VDD set to 3.3V, Load current = 0, T_A = 25°C, all tests refer to *Test Circuit* unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operation Start Voltage	V_{ST}	I_{OUT} = 1mA		0.9	1.00	V
VDD Supply Voltage	V_{DD}	VDD pin voltage	2		6	V
Shutdown Current @ I_{VIN}	I_{OFF}	CE = 0, V_{IN} = 4.5V		0.01	1	μA
Switch-off Current @ I_{VDD}	$I_{switch-off}$	V_{IN} = 6V		17	25	μA
Continuous Switching Current	I_{switch}	V_{IN} = CE = 3.3V, V_{FB} = GND		500		μA
No Load Current @ I_{VIN} (3)	$I_{no-load}$	V_{IN} = 1.5V, V_{OUT} = 3.3V		56		μA
Feedback Reference Voltage	V_{FB}	Close loop VDD = 3.3V	1.225	1.250	1.275	V
Switching Frequency	F_S	VDD = 3.3V	800	1000	1250	kHz
Maximum Duty	D_{max}	VDD = 3.3V	70	75	80	%
LX On Resistance	R_{LXon}	VDD = 3.3V		0.18	0.25	Ω
Current Limit Setting (4)	I_{limit}	VDD = 3.3V	2.3	2.5	2.7	A
Line Regulation	ΔV_{line}	V_{IN} = 3.5V ~ 6V, I_L = 1mA		0.25	5	mV/V
Load Regulation (5)	ΔV_{load}	V_{IN} = 2.5V, I_L = 1mA ~ 100mA		0.5		mV/mA
CE Pin Trip Level	V_{CEtrip}	VDD = 3.3V	0.4	0.8	1.2	V
Temperature Stability for V_{OUT}	T_S			50		ppm/°C
Thermal Shutdown Hysteresis	ΔT_{sd}			10		°C

Note 3: *No Load Current* is highly dependent on practical system design and component selection that cannot be covered by production testing. Typical *No Load Current* is verified by typical application circuit with recommended components. *No Load Current* performance is guaranteed by *Switch-off Current* and *Continuous Switching Current*.
Note 4: Current limit is guaranteed by design at T_A = 25°C.
Note 5: *Load Regulation* is not tested at production due to practical instrument limitation. *Load Regulation* performance is dominantly dependent on DC loop gain and *LX On Resistance* that are guaranteed by "*Line Regulation*" and "*LX On Resistance*" tests in production.

TEST CIRCUIT



TYPICAL APPLICATION CIRCUIT

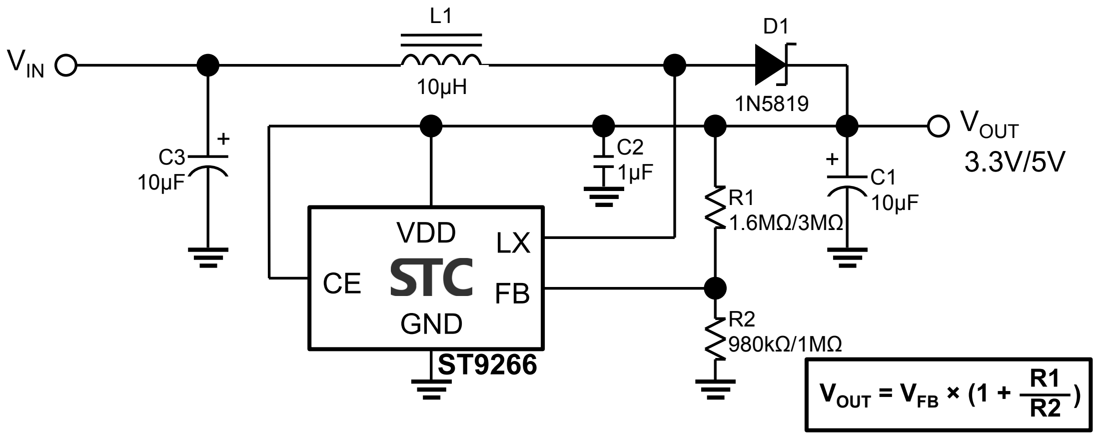


Figure 1: Typical Application for Portable Instruments

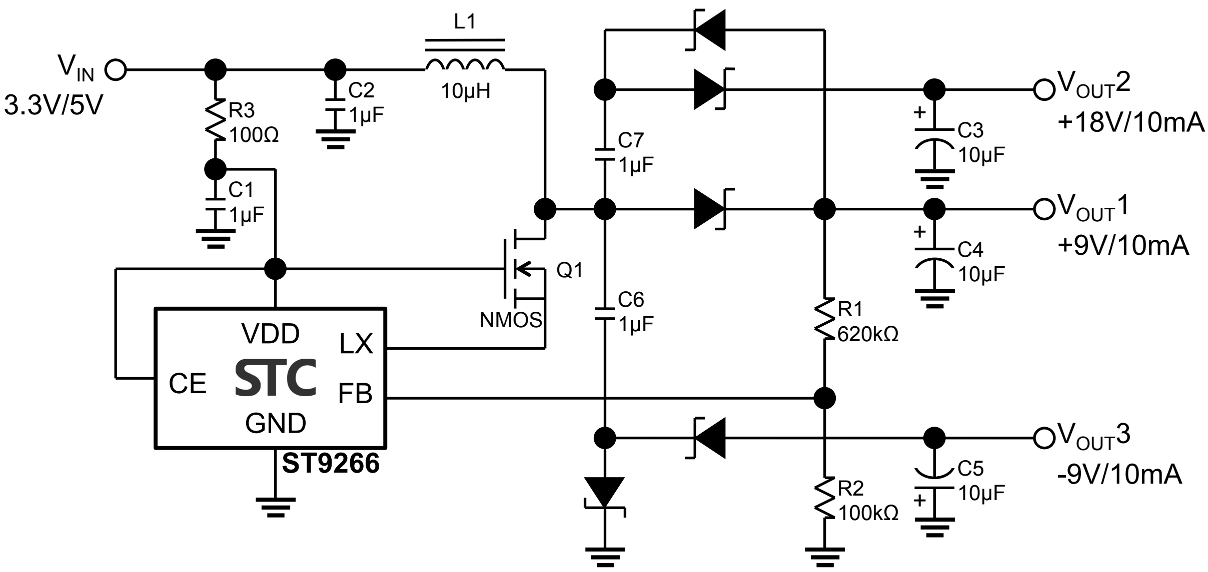
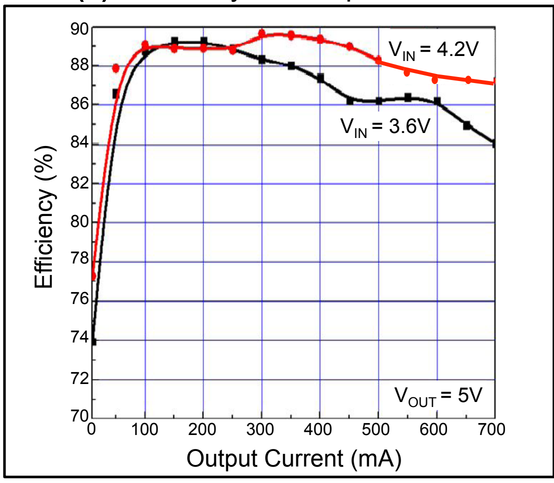


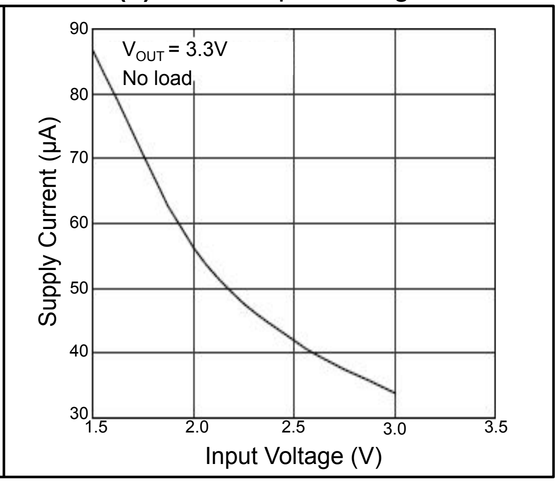
Figure 2: Multi-output Application

ELECTRICAL CHARACTERISTICS CURVES

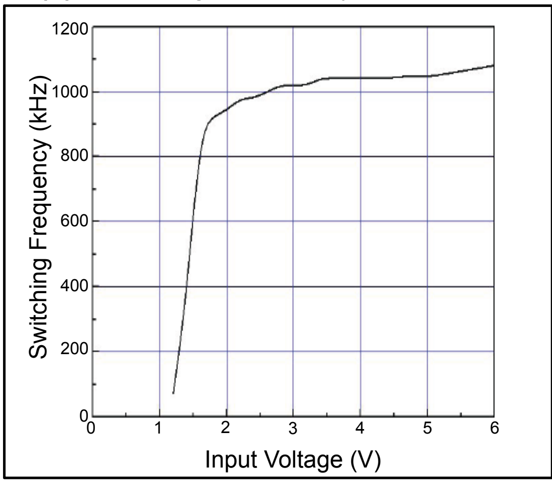
(1) Efficiency vs. Output Current



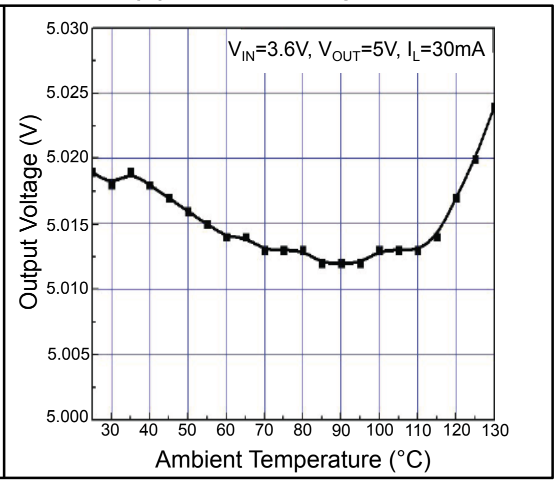
(2) I_{VIN} vs. Input Voltage



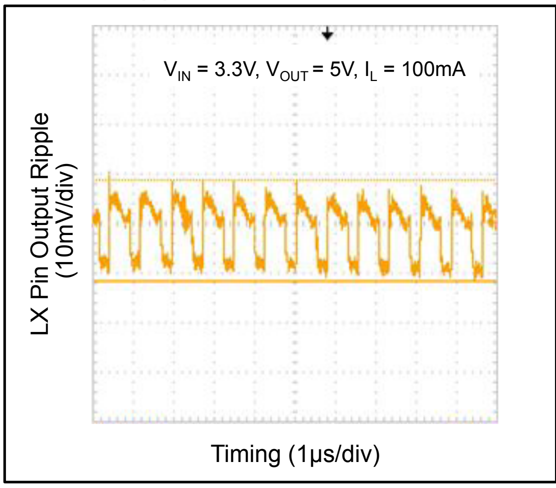
(3) Switching Frequency vs. VDD Pin



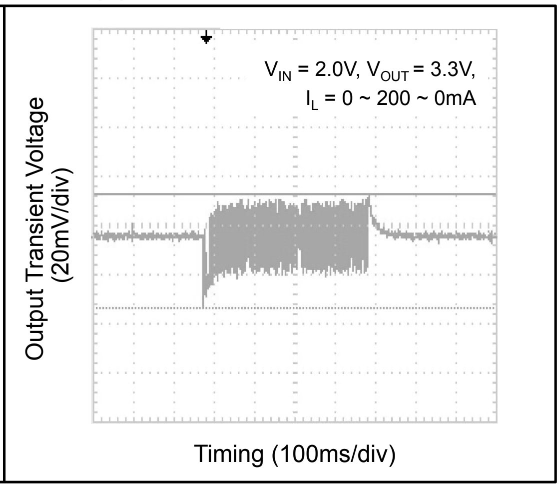
(4) Output Voltage vs. T_A



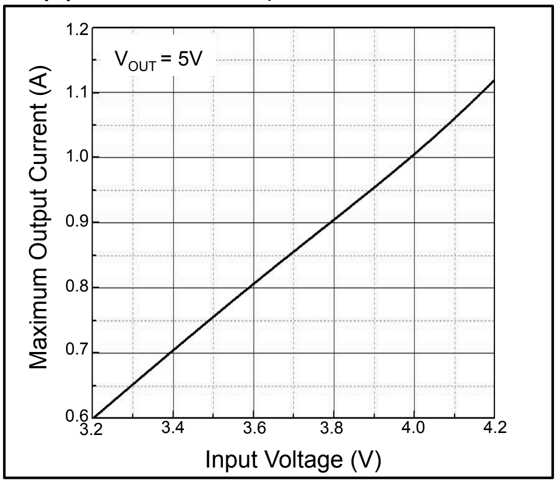
(5) LX Pin Output Ripple



(6) Output Transient Response



(7) Maximum Output Current vs. V_{IN}



APPLICATION INFORMATION

Output Voltage Setting

Referring to *Typical Application Circuit*, the output voltage of the switching regulator (V_{OUT}) can be set with Equation (1).

$$V_{OUT} = (1 + R1/R2) \times V_{FB} \quad (1)$$

Feedback Loop Design

Referring to *Typical Application Circuit*. The selection of R1 and R2 based on the trade-off between quiescent current consumption and interference immunity is stated below:

- Follow Equation (1)
- Higher R resistor reduces the quiescent current (Path current = 1.25/R2), however resistors beyond 5MΩ are not recommended.
- Lower R resistor gives better noise immunity, and is less sensitive to interference, layout parasitics, FB node leakage, and improper probing to FB pins.
- A proper value of feed forward capacitor parallel with R1 can improve the noise immunity of the feedback loops, especially in an improper layout. An empirical suggestion is around 0 ~ 33pF for feedback resistors of MΩ, and 10nF ~ 0.1μF fir feedback resistors of tens to hundreds kΩ.

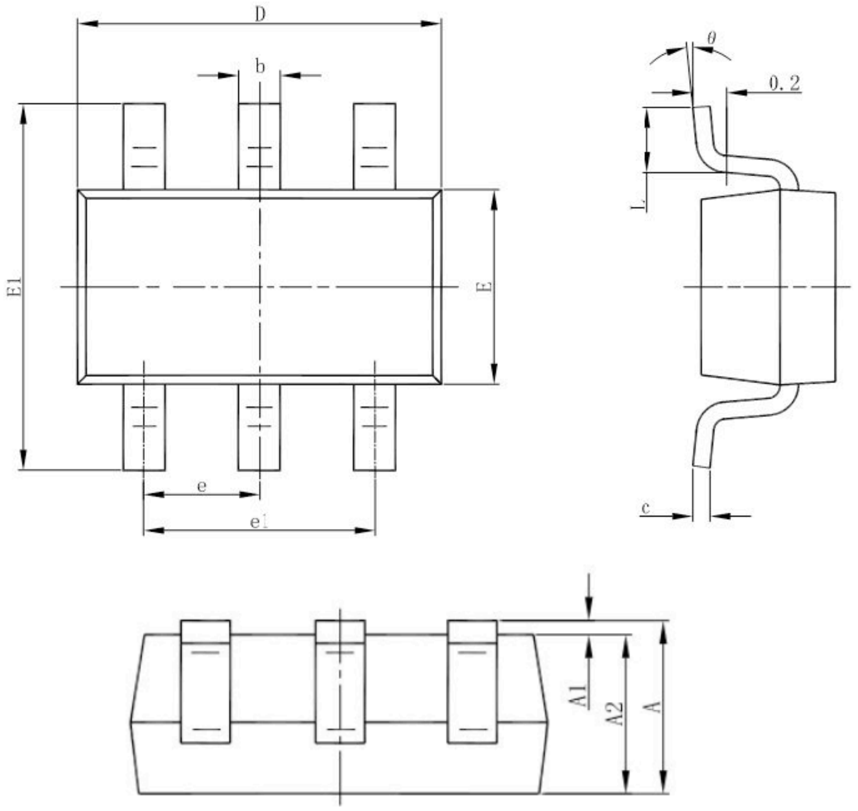
For applications without standby or suspend modes, lower values of R1 and R2 are preferred. For applications concerning the current consumption in standby or suspend modes, the higher values of R1 and R2 are needed.

Layout Guide

- A full GND plane without gap break.
- VDD to GND noise bypass – Short and wide connection for the 1μF MLCC capacitor between Pin 5 and Pin 3 (refer to SOT-23-6L pin assignment).
- V_{IN} to GND noise bypass – Add a capacitor close to L1 inductor, when V_{IN} is not an idea voltage source.
- Minimized FB node copper area and keep far away from noise source.
- Minimized parasitic capacitance connecting to LX nodes, which may cause additional switching loss.

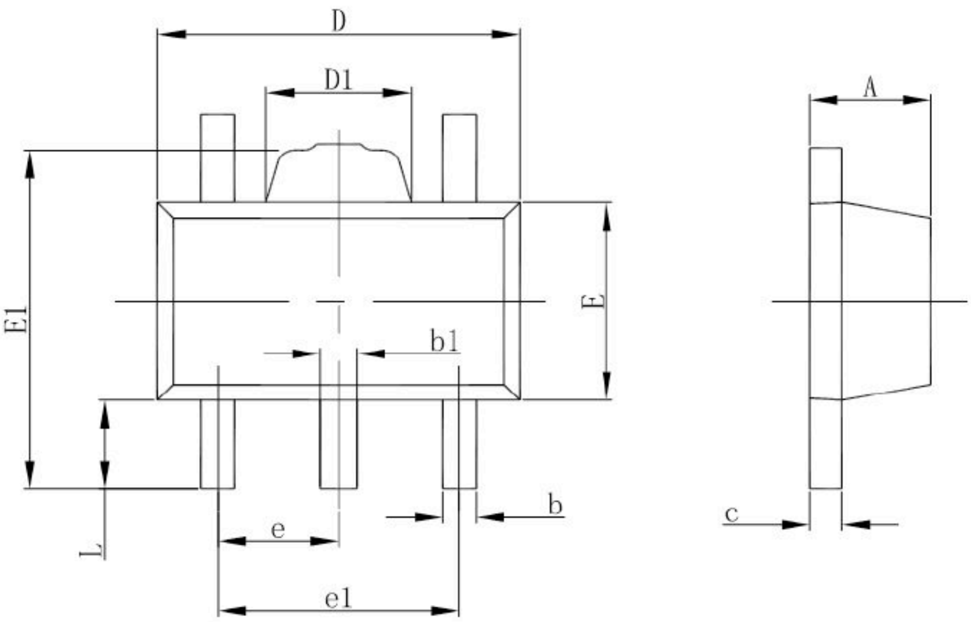
PACKAGE DIMENSION

SOT-23-6L



SYMBOL	Dimensions in Millimeters		Dimensions in Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-89-5



SYMBOL	Dimensions in Millimeters		Dimensions in Inches	
	MIN	MAX	MIN	MAX
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.360	0.560	0.014	0.022
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.400	1.800	0.055	0.071
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 (TYP)		0.060 (TYP)	
e1	2.900	3.100	0.114	0.122
L	0.900	1.100	0.035	0.043

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